ABSTRACT

A method of simultaneously forming at least one capacitor, at least one resistor and at least one metal-oxide semiconductor. A structure having: an exposed oxide structure; a capacitor region within at least a portion of the exposed oxide structure; a first resistor region within at least a portion of the exposed oxide structure; a second resistor region within at least a portion of the exposed oxide structure; and a metal-oxide semiconductor region not within at least a portion of the exposed oxide structure is provided. A first polysilicon layer is formed over the structure and the exposed oxide structure. The first polysilicon layer is doped to form a doped first polysilicon layer. An interpoly oxide film is formed over the doped first polysilicon layer. The interpoly oxide film is patterned to form: a capacitor interpoly oxide film portion within the capacitor region over the oxide structure; and a second interpoly oxide film portion within the second resistor region over the oxide structure. A second polysilicon layer is formed over the structure. The second polysilicon layer is doped to form a doped second polysilicon layer. The doped second polysilicon layer and the doped first polysilicon layer are patterned to form: within the capacitor region: a lower capacitor doped first polysilicon portion underneath at least a portion of the capacitor interpoly oxide film portion, and an overlying upper capacitor second doped polysilicon portion over at least a portion of the patterned capacitor interpoly oxide film portion; within the first resistor region: a lower first resistor first polysilicon portion and an upper, overlying first resistor second polysilicon portion; within the second resistor region: a lower second resistor first polysilicon portion underneath at least a

portion of the second interpoly oxide film portion; and within the metal-oxide semiconductor region: a lower metal-oxide semiconductor first polysilicon portion and an overlying metal-oxide semiconductor second polysilicon portion.